What Is Claimed Is:

1. A data processing device comprising a data processing logic cell field and at least one sequential CPU, wherein coupling of the sequential CPU and the data processing logic cell field for data exchange is possible in particular in block form using lines leading to a cache memory.

2. A method for operating a reconfigurable unit having runtime-limited configurations, the configurations being able to increase their maximum allowed runtime in particular by triggering a parallel counter, wherein an increase in configuration runtime by the configuration is suppressed in response to an interrupt.